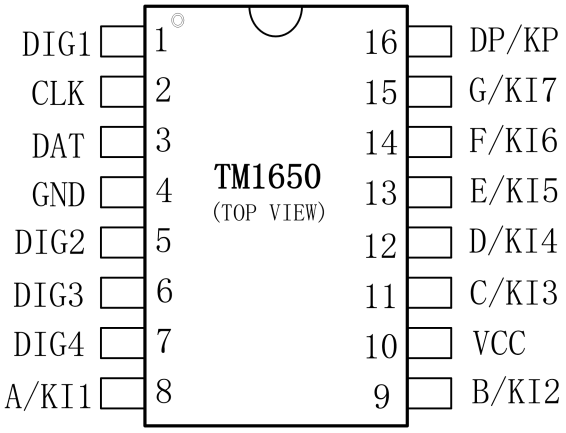
I. Overview

TM1650 is a special IC for LED (light emitting diode display) drive control with keyboard scanning interface. MCU digital interface, data latch, LED driver, keyboard scanning and other circuits are integrated inside. This product has reliable quality, good stability and strong anti-interference ability. It is mainly applicable to digital tubes such as set-top boxes, household appliances (intelligent water heaters, microwave ovens, washing machines, air conditioners, induction ovens), electronic scales, intelligent meters, etc. It can be applied to the application of 24-hour long-term continuous work.

II. Characteristic description

- Two display modes (8 segments) × 4 bits and 7 segments × (4 bits)
- Support single key 7x4bit (28 keys) and combination key (4 keys)
- Adjustable brightness level 8
- Section driving current is greater than 25mA, and bit driving current is greater than 150mA
- High speed 2-wire serial interface (CLK, DAT)
- Oscillation mode: built in RC oscillation
- Built in power on reset circuit
- Built in data latch circuit
- Support 3-5.5v supply voltage
- Strong anti-interference ability
- Packaging form: SOP16, DIP16,TSSOP16

III. Pin definition:



IV. Pin function definition:

Symbol	Pin name	No. of pin	Explain
CLK	Clock input	2	Data clock input of 2-wire serial interface with built-in pull-up resistor.
DAT	Data input / output	3	Data input or output of 2-wire serial interface with built-in open drain mode.
A/KI1-G/KI7	Scan input / output section	8-15	LED segment drive output, high level effective. Keyboard scanning input, high-level effective, built-in pull-down.
DIG1-DIG4	Bit / key sweep output	1,5 6,7	Led bit drive output, active at low level. Keyboard scanning output, high level is valid.
DP/KP	Segment output / key sweep flag output	16	Led segment drive output, high level effective. The keyboard scans the mark output. When the 7-segment screen is turned on, if a valid key is detected, the low level of the mark will be output.
VCC	Logic power supply	10	Connected to positive power supply (3-5.5v)
GND	Logical location	4	Grounding system

V. Communication sequence format:

TM1650 adopts 2-wire serial transmission protocol communication in Figure 1:

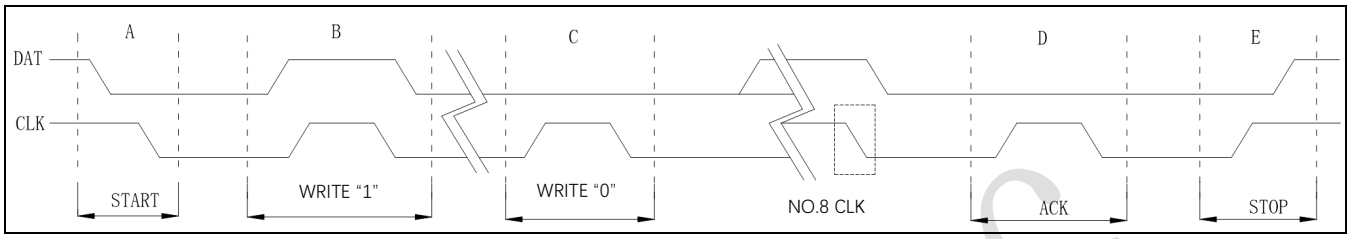


Fig. 1

1. Start signal / stop signal

Start signal: keep CLK at "1" level, and DAT jumps from "1" to "0", which is considered as the start signal. As shown in paragraph A (Figure 1);

Stop signal: keep CLK at "1" level, and DAT jumps from "0" to "1", which is considered as the stop signal. As shown in paragraph E (Figure 1);

2. ACK signal

If this communication is normal, the chip will actively pull down the DAT after the falling edge of the 8th clock of serial communication. Until the rising edge of CLK is detected, DAT is released to the input state (for the chip). As shown in paragraph D (Figure 1).

3. Write '1' and '0'

Write "1": keep DAT at "1" level, and CLK jumps from "0" to "1". If you skip from "1" to "0", it is considered to be writing "1". As shown in paragraph B (Figure 1).

Write "0": keep DAT at "0" level and CLK jumps from "0" to "1". If you skip from "1" to "0", it is considered to be writing "0". As shown in Paragraph C (Figure 1).

4. One byte (8-bit) data transmission format

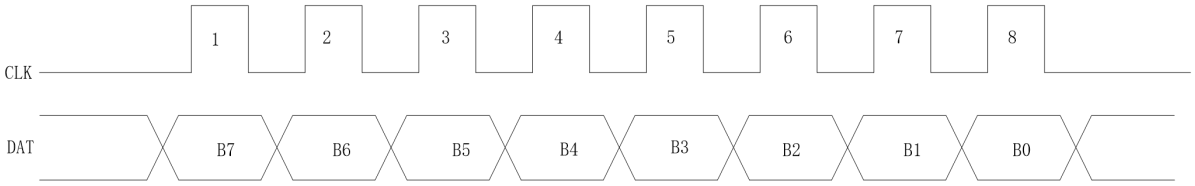


Fig. 2

The transmission format of one byte data is shown in Figure 2. When sending data, MSB is in the front and LSB is in the back, that is, the high bit is advanced. The data of microprocessor communicates with TM1650 through 2-wire serial interface. When CLK is high, the signal on DAT must remain unchanged. Only when the clock signal on CLK is low, the signal on DAT can be changed. The starting condition of data input is that CLK is at high level and DAT changes from high to low. The end condition is that when CLK is high, DAT changes from low level to high level.

5. Write display operation

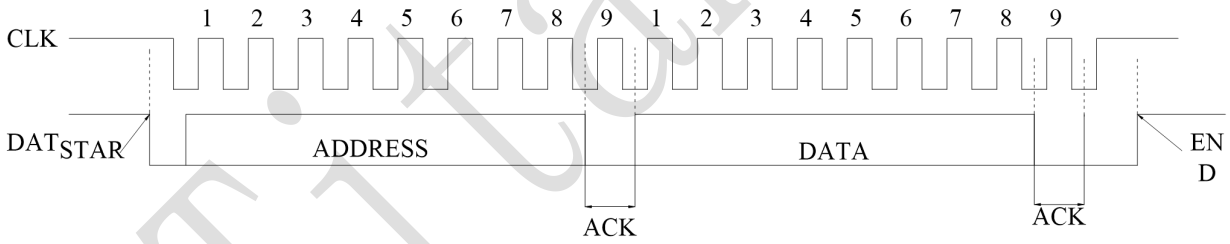


Fig. 3 Write display sequence

Address: display address (68H, 6AH, 6CH, 6EH);

Data: display data.

6. Complete operation sequence

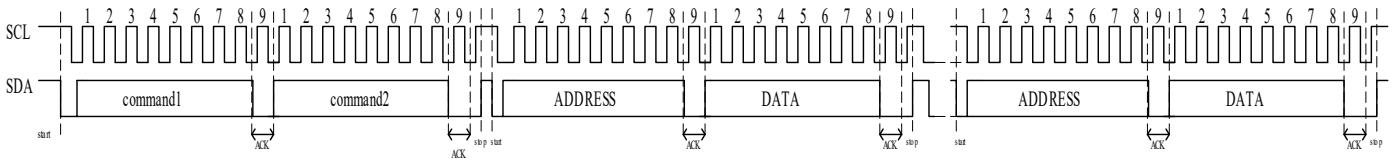


Fig. 4 Complete sequence

Command 1: system command 48H;

Command 2: system parameter setting;

Address: display address (68H, 6AH, 6CH, 6EH);

Data: display data.

Remarks:

1. Setting system parameters and writing video memory data are two independent processes. The order between them does not affect the practical application;

2. Each time you enter the system command (48H) and the system parameter setting command, the system parameters will be changed. Please pay attention to the standby command operation.

7. Read key sequence

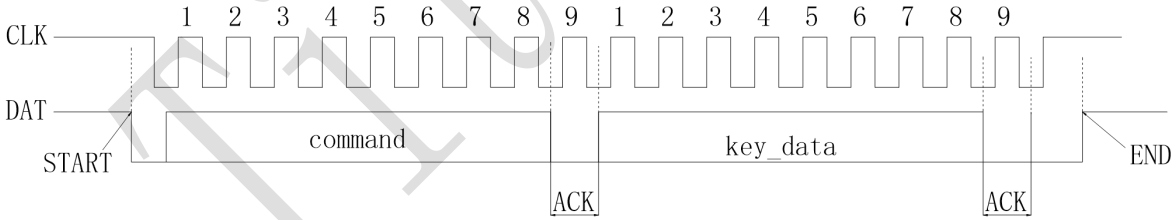


Fig. 5 Read key sequence

Command: read key command 4 FH;

Key_ data: read key data (one byte).

Remarks: when reading the key, the data is output from TM1650 to MCU. At this time, the IO port connected to the DAT of TM1650 must be set to the input mode and release the bus. Key code P7P6P5P4_P3P2P1P0 comes out first from high position (underline is easy to distinguish binary B and

hexadecimal H), and the initial state is 0010_1110B（2E). TM1650 supports single and combined keys. Key driving circuit: 2KΩ resistor shall be connected in series between DIG and KI pin. Before reading the key, the TM1650 must be in the scanning state, that is, the chip is in the on display state.

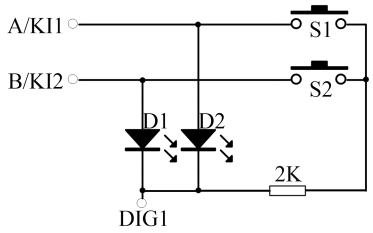


Fig. 6 Key driving circuit

Output value when the key is pressed: (P6 = 1 when the key is pressed)

KI	DIG4	DIG3	DIG2	DIG1
A/KI1	47H	46H	45H	44H
B/KI2	4FH	4EH	4DH	4CH
C/KI3	57H	56H	55H	54H
D/KI4	5FH	5EH	5DH	5CH
E/KI5	67H	66H	65H	64H
F/KI6	6FH	6EH	6DH	6CH
G/KI7	77H	76H	75H	74H
KI1+KI2	7FH	7EH	7DH	7CH

In the same DIG, the combination of KI1+KI2 is the most preferred. In addition, if multiple keys are pressed at the same time, the one with the smallest key code takes precedence. If not pressed at the same time, the first key pressed will prevail.

Keyboard scan:

1. Keyboard scanning with 28 keys of 4 * 7 matrix is supported at most. During keyboard scanning, DIG is used for column scanning output and KI is used for row scanning input.

2. Regularly insert keyboard scanning during display drive scanning. During keyboard scanning,

DIG1~DIG4 will successively output high level and other pins will output low level. At this time, KI1~KI7 output is prohibited. When no key is pressed, they are pulled down to low level. When a key is pressed, for example, the key connecting DIG2 and KI2 is pressed, KI2 inputs high level when DIG2 outputs high level. In order to avoid code errors caused by key jitter and external interference, two keyboard scans are carried out inside the chip. Only when the two scanning results are the same can the key be confirmed to be valid. Therefore, the key pressing time is greater than 2 key scanning cycles.

3. Key code is 8 bits, bit 7 (P7) is always 0, bit 2 (P2) is always 1, bit 1 and bit 0 are column scanning code, bit 5 ~ bit 3 (p5p4p3) is line scanning code, and bit 6 (P6) is status code (key press is 1, key release is 0).

For example, if the key connecting DIG2 and KI5 is pressed, the key code is 65H or 01101001B. After the key is released, that is, bit 6 (P6) is 0, and the key code is usually 25H or 00101001B (it may also be other values, but it must be less than 40H). In the following table, the column scan code corresponding to DIG1 is 01B and the row scan code corresponding to KI5 is 100b. MCU can read the key code at any time. If you need to know when the key is released, you can read the key code regularly through query until the key code bit 6 (P6) is 0.

Output value when the key is released**: (key release P6 = 0)**

KI	DIG4	DIG3	DIG2	DIG1
A/KI1	07H	06H	05H	04H
B/KI2	0FH	0EH	0DH	0CH
C/KI3	17H	16H	15H	14H
D/KI4	1FH	1EH	1DH	1CH
E/KI5	27H	26H	25H	24H
F/KI6	2FH	2EH	2DH	2CH
G/KI7	37H	36H	35H	34H
KI1+KI2	3FH	3EH	3DH	3CH

Remarks:

1. The essential difference between the key code read by the key release and the key press is whether

bit 6 (P6) is 1.

2. After the key is released, it is usually the above table, which does not rule out other situations, but it must be less than 40H.

V. Instruction set description

1. Data command settings

Name	Instructions MSB LSB								Explain	Instruction value
	B7	B6	B5	B4	B3	B2	B1	B0		
System command	0	1	0	0	1	0	0	0	Set system parameters command	48H
Read key command	0	1	0	0	1	X	X	1	Read key data command	49H

Remarks: the instruction used in this specification is hexadecimal H, and the input data and read data start from the high bit. The bit X of can be 1 or 0. It is recommended to write 0. Others must be fixed values.

2. System parameter setting

Name	Instructions MSB LSB								Explain	Instruction value
	B7	B6	B5	B4	B3	B2	B1	B0		
Brightness setting	0	0	0	0			0		Level 8 brightness (default)	00H
	0	0	0	1			0		Level 1 brightness	10H
	0	0	1	0			0		Level 2 brightness	20H
	0	0	1	1			0		Level 3 brightness	30H
	0	1	0	0			0		Level 4 brightness	40H
	0	1	0	1			0		Level 5 brightness	50H
	0	1	1	0			0		Level 6 brightness	60H

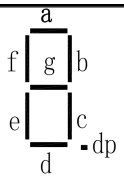
	0	1	1	1			0		Level 7 brightness	70H
Segment mode	0				0		0		8-segment output (default)	00H
	0				1		0		7-segment output	08H
Working mode	0					0	0		Normal operating mode	00H
	0					1	0		Standby mode	04H
Switch mode	0						0	0	Off screen display	00H
	0						0	1	Open screen display	01H

Remarks: before sending the above system parameter setting command, you need to input the system command 48h, such as 48h ， 10h + 01h = level 1 brightness on-screen display.

3. Video memory address

Name	Instructions								Display address value
	MSB							LSB	
	B7	B6	B5	B4	B3	B2	B1	B0	
	DP/KP	G/KI7	F/KI6	E/KI5	D/KI4	C/KI3	B/KI2	A/KI1	
DIG1	0	1	1	0	1	0	0	0	68H
DIG2	0	1	1	0	1	0	1	0	6AH
DIG3	0	1	1	0	1	1	0	0	6CH
DIG4	0	1	1	0	1	1	1	0	6EH

Remarks: according to figure 7, the common cathode drive circuit drives the 4-bit nixie tube, and dig1-dig4 display 1, 2, 3 and 4 respectively. The data to be sent by MCU is (68 + 06) + (6A+5B) + (6C+4F) + (6E+66). If you want to display 1.2.3.4, you need to set the segment mode to 8-segment output first. The data to be sent by MCU is (68 + 86) + (6A+DB) + (6C+CF) + (6E+E6). When displaying decimal, it must be in 8-segment mode.



Display data															
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
3FH	06H	5BH	4FH	66H	6DH	7DH	07H	7FH	6FH	77H	7CH	39H	5EH	79H	71H
0.	**1.**	**2.**	**3.**	**4.**	**5.**	**6.**	**7.**	**8.**	**9.**	**A.**	**B.**	**C.**	**D.**	**E.**	**F.**
BFH	86H	DBH	CFH	E6H	EDH	FDH	87H	FFH	DFH	F7H	FCH	B9H	DEH	F9H	F1H

4. Segment mode and key indication

8-segment mode: DP / KP and KI1-KI7 have the same function and are output as segments. It can drive LED or digital tube;

7-segment mode: KI1-KI7 is used as segment output, which can drive LED or nixie tube, and DP / KP pin is used as key scanning mark output. When the screen is turned on in 7-segment mode (48H+09H), DP / KP pin outputs high level when no key is pressed. When a key is pressed, DP / KP pin will output low level. After the next key data is read (or the screen is closed), DP / KP pin outputs high level.

5. Standby and wake up

Standby: as long as the value of bit 2 (B2) in the system parameter setting command is 1, the chip will enter the standby mode. In standby mode, the chip stops working, but the display data inside the chip will not change;

Wake up: after the chip enters the standby mode, it can wake up in the following ways:

1. Send a non standby mode system parameter setting instruction, such as 48H+01H (8-level brightness + normal mode + 8-segment mode + on display). Its essence is to make the system parameter setting instruction bit 2 (B2) not 0;

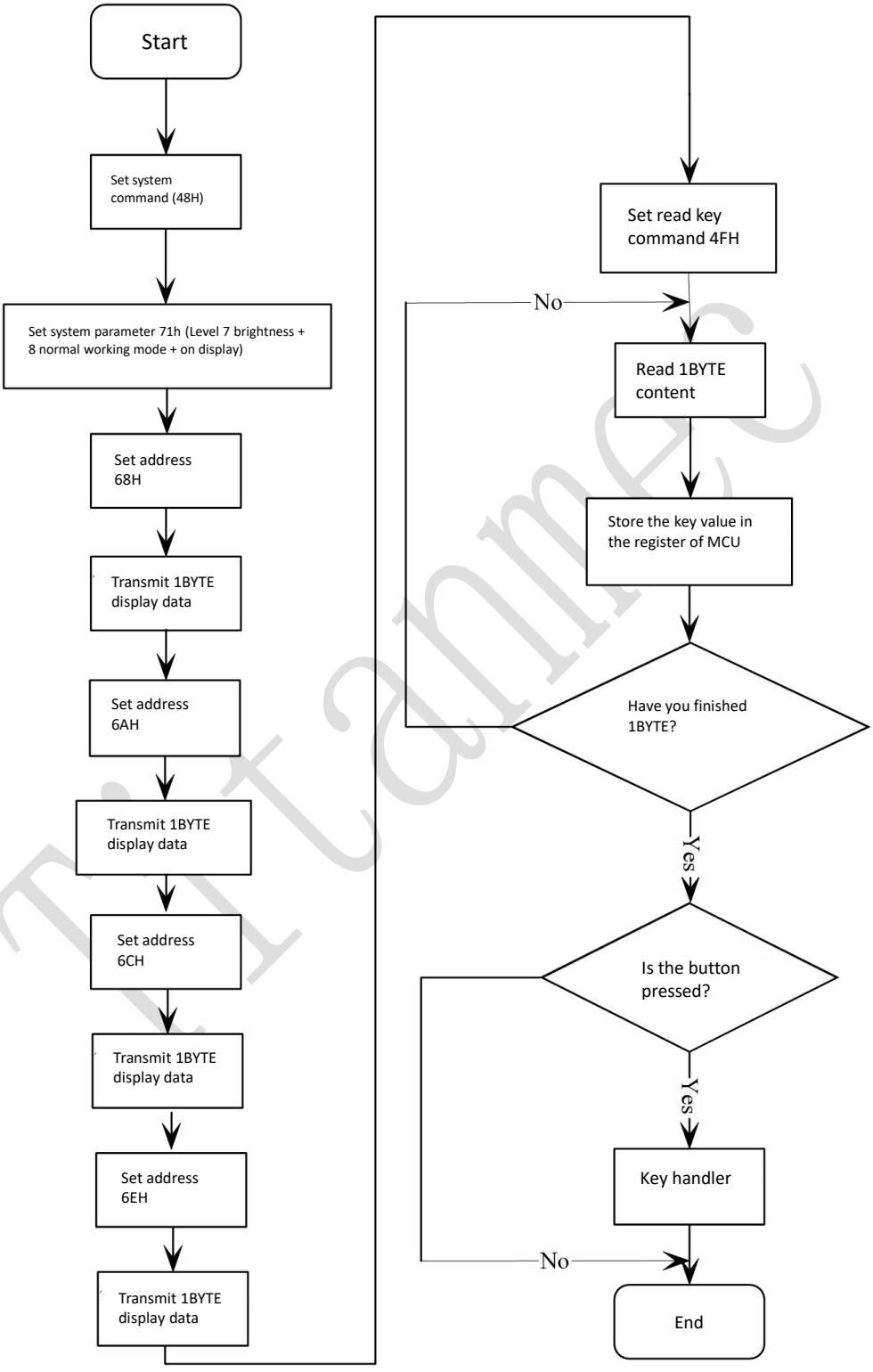
2. The chip can be awakened by the key composed of KI1-KI4 and DIG1-DIG4. The time of pressing the key must be greater than 2 key scanning cycles (80ms). Note that it is impossible to observe whether the key can wake up when the screen is turned off. Therefore, when using the key to wake up, please use the standby command, such as 48H+45H (Level 4 brightness + standby mode + on display).

6. On and off screen

On screen: when the screen opening command is sent and it is in the normal working mode, DIG1-DIG4 starts scanning;

Off screen: when the off screen command is sent, the chip stops working. After the screen is turned on, the chip needs to be initialized again;

VI. Complete operation flow chart:



Remarks: set system parameters. Customers can set them according to their actual needs.

VII. Application circuit:

Hardware circuit diagram of tm1650 driving common cathode digital screen 6:

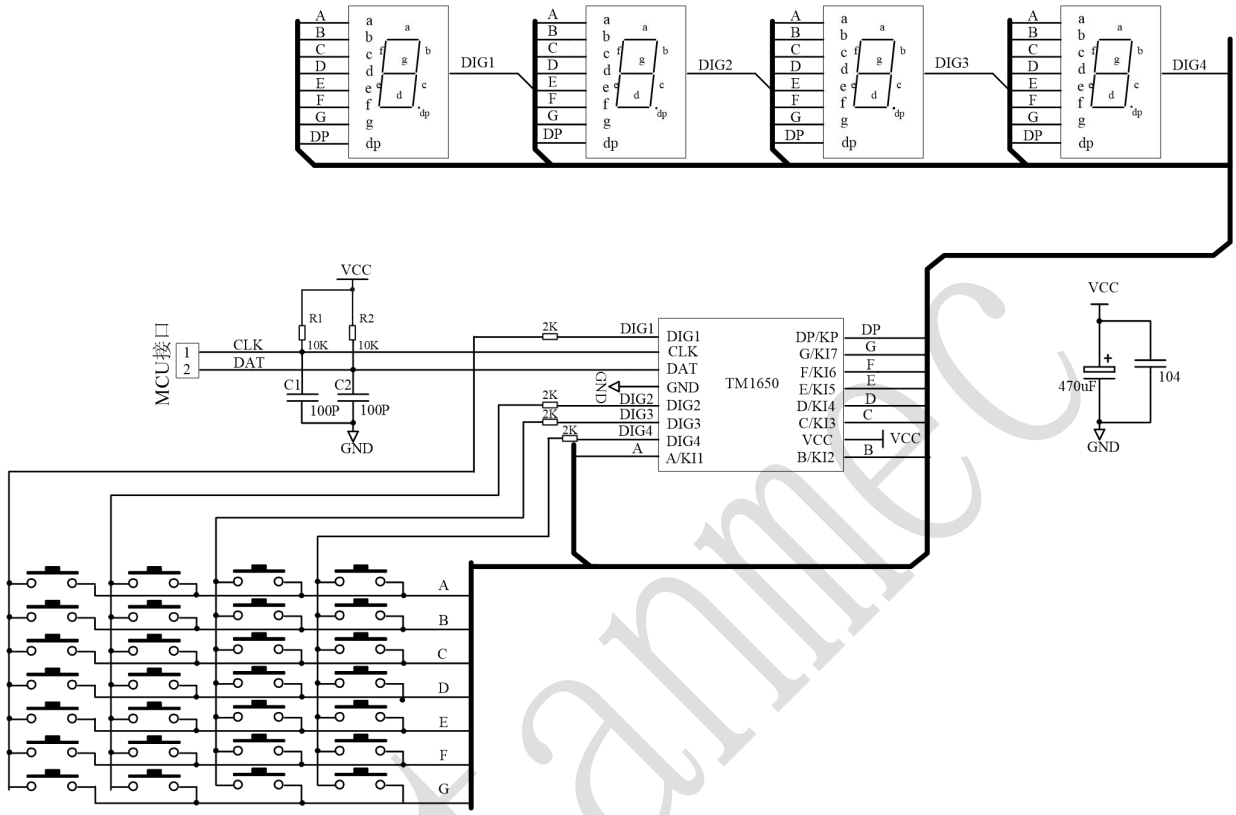


Fig.7 Common cathode drive circuit

▲ Remarks:

1. The filter capacitor between VDD and GND shall be placed close to TM1650 chip as far as possible in PCB wiring to enhance the filtering effect. Try to reduce the loop area of power supply and ground network, and provide wiring of no less than 0.5mm for power supply and ground network.

2. DAT and CLK ports must be connected with pull-down capacitor, and 100pF is recommended. The pull-up resistor must be connected, which is recommended to be 10K Ω.

3. The turn-on voltage and step-down voltage of blue light nixie tube is about 3V, so 5V should be selected for TM1650 power supply.

4. When the chip works in strong interference environment such as induction cooker, it is recommended to appropriately reduce the communication frequency between TM1650 and MCU, and

100 Ω resistance can be connected in series on the communication port.

VIII. Electrical parameters:

Limit parameters（Ta = 25℃）

Parameter	Symbol	Range	Unit
Logic supply voltage	VDD	-0.5 ～+6.5	V
Logic input voltage	VI1	-0.5 ～ VDD + 0.5	V
Led segment drive output current	IO1	0 ～ 30	mA
Led bit drive output current	IO2	0 ～ 150	mA
Working temperature	Topt	-40 ～ +85	℃
Storage temperature	Tstg	-65 ～+125	℃

Electrical characteristics (test conditions: Ta=25℃，VCC=5V）

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	VCC	3	5	5.5	V
Supply current	Ic	0.2	80	150	mA
Quiescent current (CLK, DAT, KP are high level)	Ic_S	-	0.3	0.6	mA
Standby current (CLK, DAT, KP are high level)	Ist	-	0.05	0.1	mA
Low level input voltage of CLK and dat pins	VIL	-0.5	-	0.8	V
High level input voltage of CLK and dat pins	VIH	2.2	-	VCC+0.5	V
KI pin low level input voltage	VIL(KI)	-0.5	-	0.5	V
KI pin high level input voltage	VIH(KI)	1.8	-	VCC+0.5	V
Low level output voltage of dig pin (- 200mA)	VOL(DIG)	-	-	1.2	V
Low level output voltage of dig pin (- 100mA)	VOL(DIG)	-	-	0.8	V
High level output voltage of dig pin (5mA)	VOH(DIG	4.5	-	-	V

	)				
KI pin low level output voltage (-20mA)	VOL(KI)	-	-	0.5	V
KI pin high level output voltage (20mA)	VOH(KI)	4.5	-	-	V
Low level output voltage of other pins (- 4mA)	VOL	-	-	0.5	V
High level output voltage of other pins (4mA)	VOH	4.5	-	-	
KI pin input pull-down current	IDN1	-30	-50	-90	uA
CLK pin input pull-up current	IUP1	10	200	300	uA
DAT pin input pull-up current	IUP2	150	300	400	uA
KP pin output pull-up current	IUP3	500	2000	5000	uA
Default voltage threshold for power on reset	VR	2.3	2.6	2.9	V

Internal timing parameters (test conditions: Ta=25℃，VCC=5V）

Parameter	Symbol	Min	Typical	Max	Unit
Reset time generated by power on detection	TPR	10	25	60	ms
Display scan cycle	TP	4	8	20	ms
Keyboard scanning interval, key response time	TKS	20	40	80	ms

Remarks: the timing parameters in this table are multiples of the built-in clock cycle, and the built-in clock frequency decreases with the decrease of power supply voltage.。

temporal characteristic（Ta = 25℃,VCC = 5V）

Parameter	Symbol	Min	Typical	Max	Unit
Establishment time of DAT falling edge start signal	TSSTA	100	-	-	ns
Holding time of DAT falling edge start signal	THSTA	100	-	-	ns
Establishment time of DAT rising edge	TSST0	100	-	-	ns

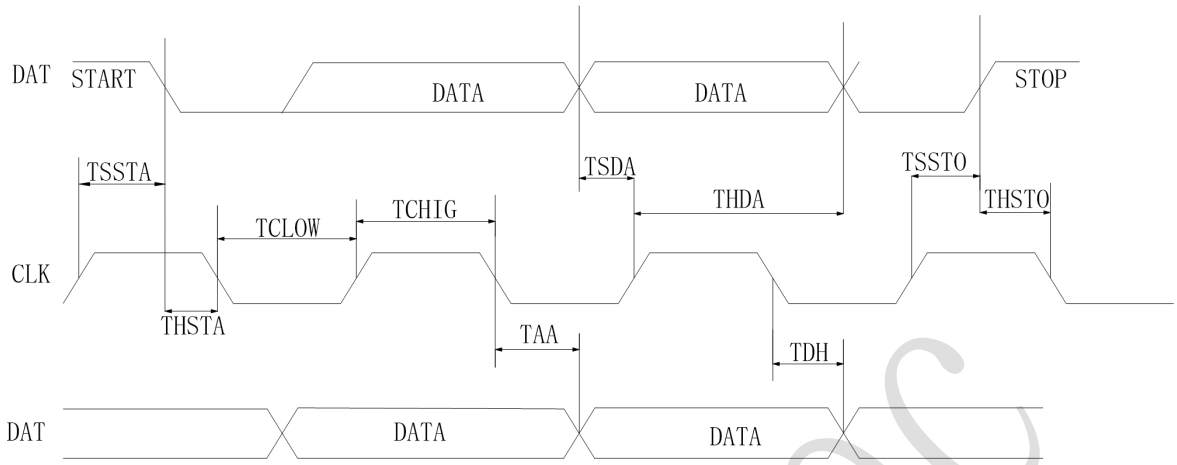
stop signal					
Holding time of DAT rising edge stop signal	THST0	100	-	-	ns
Low level width of CLK clock signal	TCLOW	100	-	-	ns
High level width of CLK clock signal	TCHIG	100	-	-	ns
Establishment time of DAT input data to the rising edge of CLK	TSDA	30	-	-	ns
Holding time of DAT input data to the rising edge of CLK	THDA	10	-	-	ns
The falling edge of the delay CLK is valid for the output data	TAA	2	-	30	ns
Delay of CLK falling edge due to invalid dat output data	TDH	2	-	40	ns
Average data transmission rate	Rate	0	-	4M	bps

Remarks:

1. The unit of measurement in this table is nanosecond, i.e. 10^{-9}. If the maximum value is not indicated, the theoretical value can be infinite.

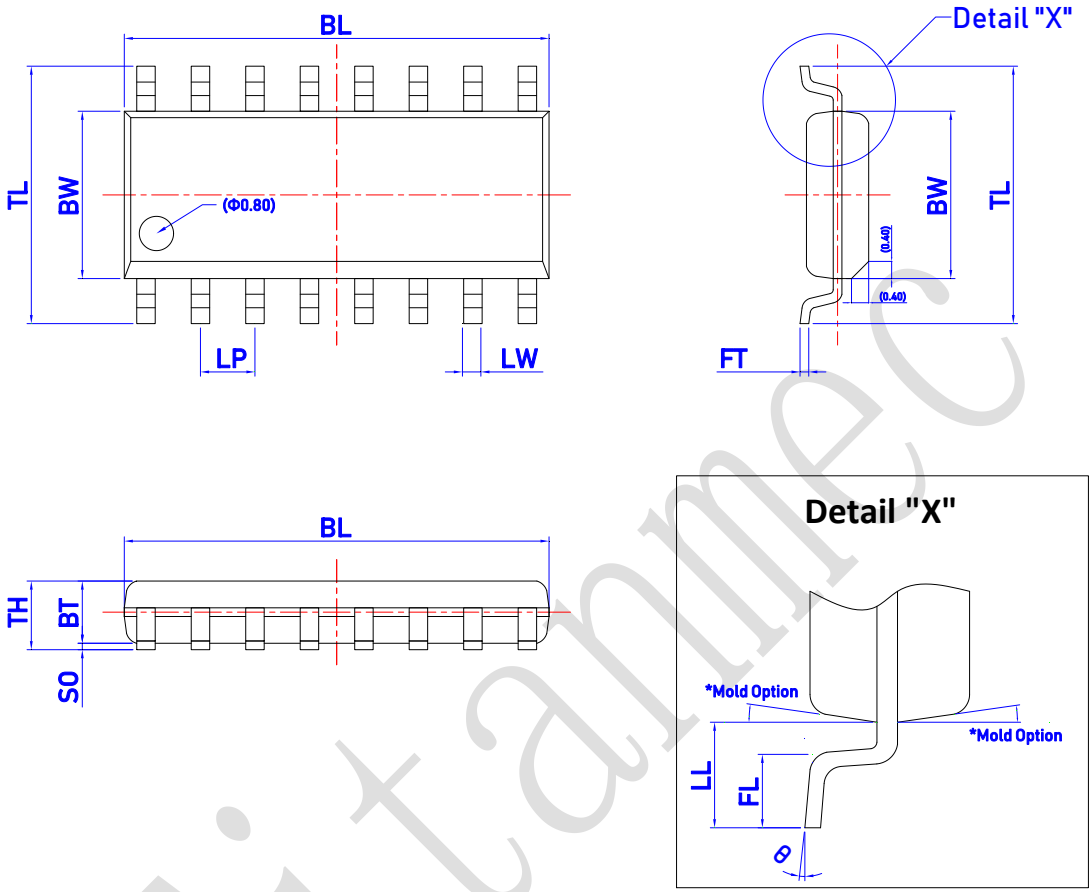
2. For different host computer platforms and hardware interface configurations, the average data transmission rate will vary greatly. The recommended value is below 100kHz.

Timing waveform：



IX. Schematic diagram of IC package：

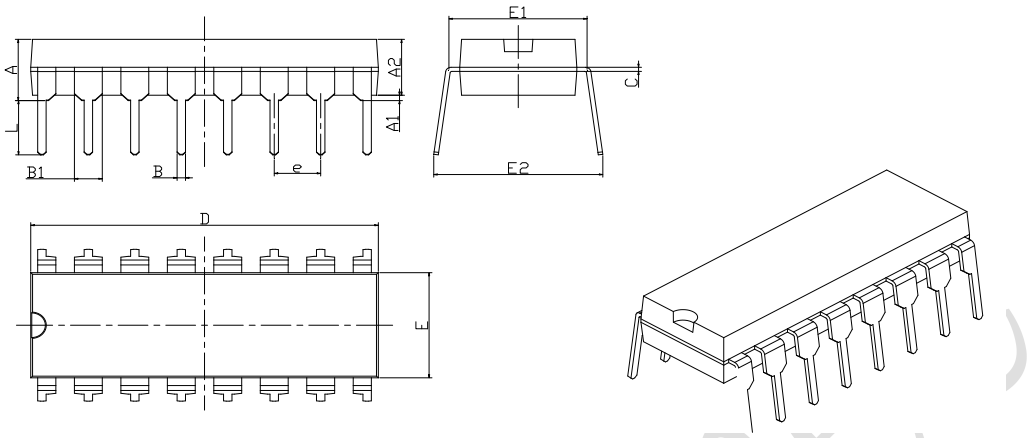
SOP16-150 Package size



Dimensions

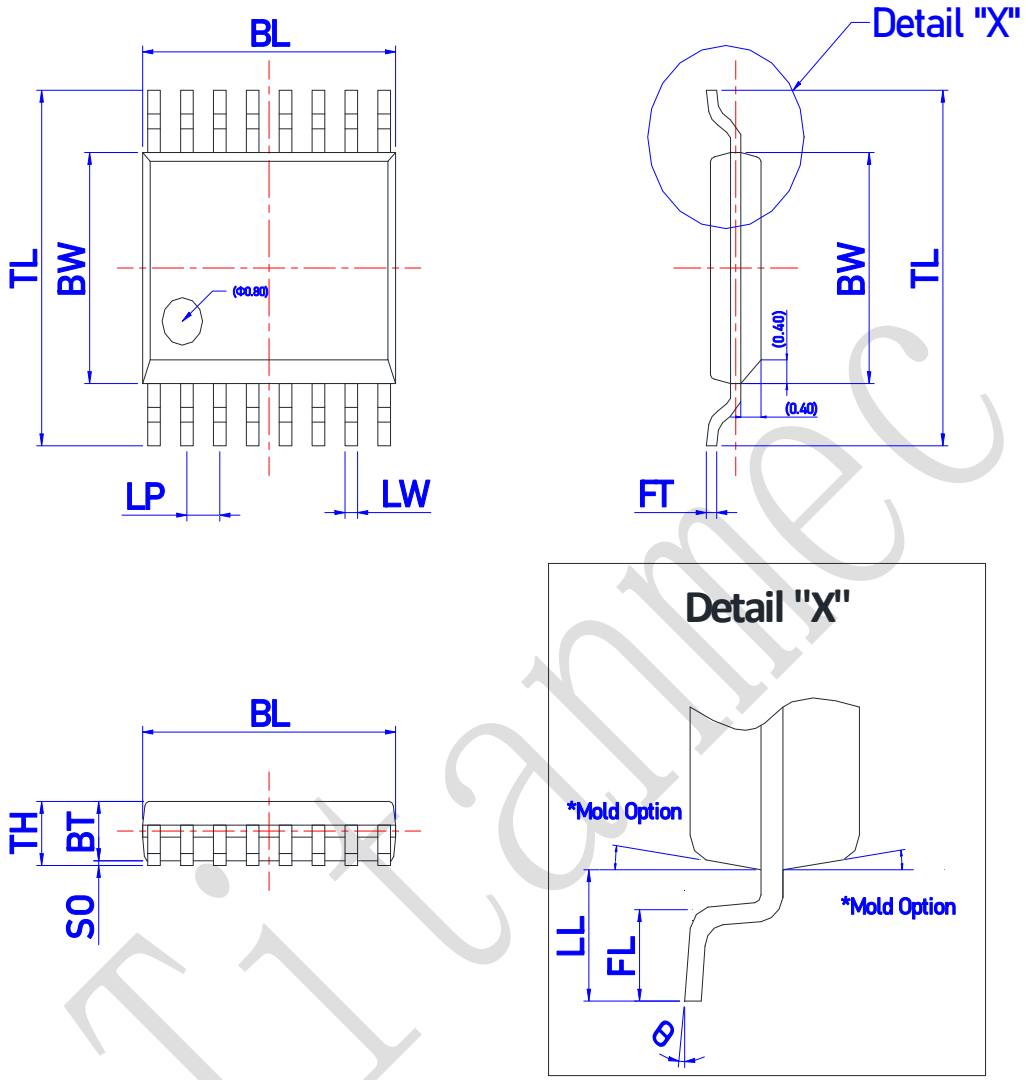
Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	10.00 (9.90) 9.80	4.00 (3.90) 3.80	6.20 (6.00) 5.80	0.430 TYP	1.270 TYP	0.250 (0.200) 0.150	1.55 (1.45) 1.25	0.200 (0.150) 0.060	1.650 Max.	1.25 (1.04) 0.80	0.80 (0.60) 0.45	8 (4) 0

DIP16 Package size



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

TSSOP16-150 Package size



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
表示	总长	胶体宽度	跨度	脚宽	脚间距	脚厚	胶体厚度	站高	胶体高度	单边长	脚长	脚角度
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	5.05 (5.00) 4.95	4.00 (3.90) 3.80	6.30 (6.00) 5.70	0.250 TYP	0.650 TYP	0.250 (0.200) 0.150	1.05 (1.00) 0.95	0.100 (0.080) 0.020	1.100 Max.	1.25 (1.05) 0.85	0.85 (0.65) 0.40	8 (4) 0

All specs and applications shown above subject to change without prior notice.