CHIPSEA CS1232

24-bit Sigma-Delta Analog-to-Digital Converter (ADC)

User Manual
Revision 1.5
Chipsea Technologies

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Revision History

Revision	Description of Changes	Date
REV 1.0	Initial release version.	2011-08-25
REV 1.1	Updated clock description, added temperature sensor details.	2011-09-20
REV 1.2	Updated package information.	2011-11-30
REV 1.3	Updated electrical characteristics table.	2012-05-20
REV 1.4	Modified AD value read timing: 25th SCLK pulls DRDY high.	2012-07-09
REV 1.5	Updated company LOGO and re-released document.	2014-10-17

1. General Description

The CS1232 is a high-precision, low-power analog-to-digital converter (ADC). It features 24-bit resolution with an effective number of bits (ENOB) up to 20.8 bits. The chip is widely applicable in industrial process control, electronic scales, liquid/gas chemical analysis, blood analyzers, smart transmitters, and portable measurement instruments.

1.1 Key Features

- Integrated low-noise PGA with selectable gains: 1, 2, 64, 128
- Integrated 2-channel 24-bit no-missing-codes differential input ADC; ENOB reaches 20.8 bits at PGA=128
- P-P Noise: 139 nV at 10Hz; 298 nV at 80Hz
- Integrated RC oscillator (±8%), supports external crystal or external clock input
- Selectable output rate: 10Hz or 80Hz
- Integrated 2-wire SPI serial communication interface
- Integrated internal temperature sensor
- Integral Non-Linearity (INL) < 0.001%

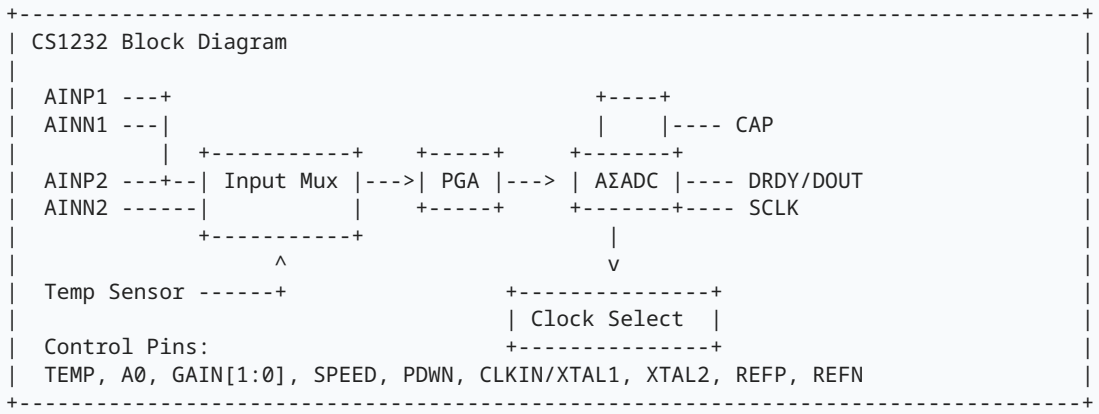
1.2 Applications

- Industrial Process Control
- Electronic Scales & Weighing Systems
- Liquid / Gas Chemical Analysis
- Blood Meters / Medical Instruments

- Smart Transmitters
- Portable Instrumentation

1.3 Basic Structural Description

The CS1232 includes a 3rd-order Sigma-Delta modulator and a low-noise instrumentation amplifier structure for PGA amplification. When PGA=128, effective resolution reaches 20.8 bits. Output rates are selectable at 10Hz or 80Hz. In addition to the built-in RC oscillator, external crystals or clock sources via the CLKIN/XTAL1 pin are supported. Low-power operational modes including Standby and Power Down are integrated.



1.4 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	AVDD	-0.3	6	V
Digital Supply Voltage	DVDD	-0.3	6	V
Voltage Difference (AGND to DGND)	-	-0.3	0.3	V
Transient Supply Current	-	-	100	mA
Continuous Supply Current	-	-	10	mA
Digital Input Voltage	-	-0.3	DVDD + 0.3	V
Analog Input Voltage	-	-0.3	AVDD + 0.3	V
Junction Temperature	-	-	150	°C
Operating Temperature Range	-	-40	105	°C
Storage Temperature Range	-	-60	150	°C
Lead Soldering Temperature	-	-	240	°C

1.5 Digital Logic Characteristics

Table 2: Digital Logic Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions / Notes
VIH (High Level Input Voltage)	0.7 × DVDD	-	DVDD + 0.1	V	Standard Digital Inputs
VIL (Low Level Input Voltage)	DGND	-	0.3 × DVDD	V	Standard Digital Inputs
VIH (PDWN Pin)	0.8 × DVDD	-	DVDD + 0.1	V	PDWN Pin
VIL (PDWN Pin)	DGND	-	0.2 × DVDD	V	PDWN Pin
VOH (High Level Output Voltage)	DVDD - 0.4	-	DVDD	V	IOH = 1 mA
VOL (Low Level Output Voltage)	DGND	-	0.2 × DVDD	V	IOL = 1 mA
IIH (Input High Current)	-	-	10	µA	VI = DVDD
IIL (Input Low Current)	-10	-	-	µA	VI = DGND
External Clock Frequency Range	0.2	4.9152	8	MHz	Chip system clock
Serial Clock (SCLK) Frequency	-	-	2	MHz	SPI serial interface clock

1.6 Electrical Characteristics

All parameters tested at ambient temperature -20°C to +85°C, AVDD = DVDD = 5V (or 3V as specified), REFP = AVDD, REFN = 0V unless otherwise noted.

Table 3: Electrical Characteristics (AVDD = DVDD = 5V)

Parameter	Conditions	Min	Typ	Max	Unit
Analog Inputs					
Full-Scale Input Range (AINP - AINN)	-	-	±0.5 VREF / PGA	-	V
Common Mode Input Range	PGA = 1, 2	AGND - 0.1	-	AVDD + 0.1	V
	PGA = 64, 128	AGND + 1.5	-	AVDD - 1.5	V
CMRR (Common Mode Rejection)	-	-	125	-	dB
Differential Input Impedance	All Gain Settings	-	> 1	-	GΩ
System Performance					
Resolution	No missing codes	-	24	-	Bits
ADC Data Rate	Clock = 4.9152 MHz	-	10 / 80	-	Hz
Settling Time	Full settling	-	4	-	Conversion Cycles
Peak-to-Peak Noise	PGA = 128, DR = 10Hz	-	139	-	nV
Integral Non-Linearity (INL)	PGA = 128	-	±6	-	ppm
Offset Error	PGA = 128	-	-1	-	µV

Parameter	Conditions	Min	Typ	Max	Unit
Offset Drift	PGA = 128	-	25	-	nV/°C
Gain Error	PGA = 128	-	±0.1	-	%
Gain Error Drift	PGA = 128	-	6	-	ppm/°C
Reference Voltage Input					
Negative Reference Voltage (REFN)	-	AGND - 0.1	-	AGND + 0.6	V
Positive Reference Voltage (REFP)	-	REFN + 2.5	-	AVDD + 0.1	V
Reference Voltage Span (REFP - REFN)	-	2.5	AVDD	AVDD + 0.1	V
PSRR (Power Supply Rejection)	PGA = 64, 128	-	110	-	dB
Power Supply & Current Consumption					
Analog Operating Voltage (AVDD)	-	2.8	5.0	5.5	V
Digital Operating Voltage (DVDD)	-	2.8	5.0	5.5	V
Analog Supply Current	Normal (PGA = 1, 2)	-	2.0	-	mA
	Normal (PGA = 64, 128)	-	3.0	-	mA
	Standby Mode	-	6.0	-	µA
	Power Down Mode	-	0.1	-	µA
Digital Supply Current	Normal Mode	-	400	-	µA
	Standby Mode	-	150	-	µA
	Power Down Mode	-	1.5	-	µA

Table 4: Electrical Characteristics (AVDD = DVDD = 3V)

Parameter	Conditions	Min	Typ	Max	Unit
Full-Scale Input Range (AINP - AINN)	-	-	±0.5 VREF / PGA	-	V
Peak-to-Peak Noise	PGA = 128, DR = 10Hz	-	145	-	nV
INL	PGA = 128	-	±6	-	ppm
Reference Voltage Span (REFP - REFN)	-	1.5	AVDD	AVDD + 0.1	V
Analog Current (PGA = 1, 2)	Normal Mode	-	1.8	-	mA
Analog Current (PGA = 64, 128)	Normal Mode	-	2.7	-	mA
Digital Current	Normal Mode	-	360	-	µA

1.7 Noise Performance

Table 5: Noise Performance Specifications

Conditions	Data Rate	Gain	RMS Noise	P-P Noise	ENOB (RMS)	Noise-Free Bits
AVDD = 5V VREF = 5V	10 Hz	1	400 nV	1.69 µV	23.6	21.5
		2	278 nV	900 nV	23.1	21.4
		64	23 nV	149 nV	21.7	19.0
		128	21 nV	139 nV	20.8	18.1
	80 Hz	1	1.57 µV	9.53 µV	21.6	19.0
		2	903 nV	5.87 µV	21.4	18.7
		64	56 nV	342 nV	20.4	17.8
		128	56 nV	298 nV	19.4	17.0
AVDD = 3V VREF = 3V	10 Hz	1	334 nV	2.02 µV	23.1	20.5
		2	291 nV	1.43 µV	22.3	20.0
		64	26 nV	167 nV	20.8	18.1
		128	23 nV	145 nV	20.0	17.3
	80 Hz	1	2.02 µV	11.44 µV	20.5	18.0
		2	943 nV	5.34 µV	20.6	18.1
		64	63 nV	383 nV	19.5	16.9
		128	67 nV	358 nV	18.4	16.0

1.8 Pin Configurations

Table 6: Pin Description

Pin No.	Name	Type	Description
1	DVDD	Power	Digital Power Supply
2	DGND	Power	Digital Ground
3	CLKIN / XTAL1	Digital Input	External Crystal Port / External Clock Input
4	XTAL2	Digital Input	External Crystal Port
5, 6	DGND	Power	Digital Ground
7	TEMP	Digital Input	Internal Temperature Sensor Control: 0 = Disable, 1 = Enable
8	A0	Analog Input	Channel Select: 0 = Select Channel 1, 1 = Select Channel 2
9, 10	CAP1, CAP2	Analog Input	PGA Output Ports; Connect a 0.1 µF external capacitor between CAP1 and CAP2
11	AINP1	Analog Input	Channel 1 Positive Differential Input
12	AINN1	Analog Input	Channel 1 Negative Differential Input
13	AINN2	Analog Input	Channel 2 Negative Differential Input

Pin No.	Name	Type	Description
14	AINP2	Analog Input	Channel 2 Positive Differential Input
15	REFN	Analog Input	Negative Reference Input
16	REFP	Analog Input	Positive Reference Input
17	AGND	Power	Analog Ground
18	AVDD	Power	Analog Power Supply
19	GAIN0	Analog Input	PGA Gain Selection Pins: GAIN1=0, GAIN0=0 → Gain = 1 GAIN1=0, GAIN0=1 → Gain = 2 GAIN1=1, GAIN0=0 → Gain = 64 GAIN1=1, GAIN0=1 → Gain = 128
20	GAIN1	Analog Input	
21	SPEED	Digital Input	Output Data Rate Selection: 0 = 10Hz; 1 = 80Hz
22	PDWN	Digital Input	Power Down Control Pin (Active Low)
23	SCLK	Digital Input	SPI Serial Clock Input
24	DRDY / DOUT	Digital Output	SPI Data Ready / Serial Data Output Pin

2. Functional Module Description

2.1 Analog Input Front-End

The CS1232 contains a single ADC integrated with a 2-channel differential input multiplexer. Signals can be routed from differential pairs (AINP1/AINN1 or AINP2/AINN2) or from the internal temperature sensor. Input channel selection is controlled by pin A0, while temperature sensor selection is enabled via the TEMP pin.

2.2 Temperature Sensor

The chip includes an internal temperature measurement capability. When the TEMP pin is set HIGH, the ADC input connects to the internal temperature sensor, bypassing other analog inputs. When TEMP=1, the ADC only supports PGA settings of 1 or 2 (GAIN0=0 selects PGA=1; GAIN0=1 selects PGA=2).

> **Temperature Calibration Formula:**
> Single-point calibration is required. If code Y_a is measured at known temperature point A (°C), the temperature at any measured code Y_b is calculated as:
>
> $$Temperature\ (°C) = Y_b \times (273.15 + A) / Y_a - 273.15$$

2.3 Low-Noise PGA Amplifier

The low-noise PGA connects directly to bridge sensors. An integrated front-end anti-EMI filter ($R = 450\ \Omega$, $C = 18\ pF$) provides 20MHz high-frequency filtering. When PGA=1 or 2, the 64x PGA stage is bypassed/powered down to save power. An external 0.1 µF capacitor across the CAP1/CAP2 pins interacts with internal 2 kΩ resistors (R_{INT}) to form a low-pass anti-aliasing filter.

2.4 Clock Source

The CS1232 can operate using an internal RC oscillator, an external crystal oscillator, or an external clock signal. The integrated *CLK_DETECT* module monitors external clocks. If the clock frequency on CLKIN/XTAL1 exceeds

200kHz, the internal oscillator is automatically disabled. When using the internal oscillator, CLKIN/XTAL1 should be tied LOW.

2.5 Reset and Power Down

Upon power-up, internal Power-On Reset (POR) circuits initialize the chip. Pulling the ***PDWN*** pin LOW enters Power Down mode, reducing current draw below 1.6 µA. For normal operation, ***PDWN*** must be held HIGH.

2.6 SPI Serial Interface

The 2-wire SPI interface uses SCLK and ***DRDY / DOUT***. When ***DRDY / DOUT*** transitions LOW, new conversion data is ready. Clocking SCLK shifts out 24-bit data starting with MSB. A 25th SCLK pulse forces ***DRDY / DOUT*** back HIGH.

Table 7: SPI Timing Specifications

Symbol	Description	Min	Typ	Max	Unit
t2	DRDY/DOUT low to 1st SCLK rising edge	0	-	-	ns
t3	SCLK high or low pulse width	250	-	-	ns
t4	SCLK rising edge to new data bit valid (propagation delay)	-	-	200	ns
t5	SCLK rising edge to old data bit invalid (hold time)	0	-	-	ns
t6	Data update period (reading prohibited)	39	-	-	µs
t7	Conversion time (SPEED = 1, 80Hz)	-	12.5	-	ms
	Conversion time (SPEED = 0, 10Hz)	-	100	-	ms

2.7 Data Format

Data is output in 24-bit 2's complement binary format (MSB first). The LSB size equals ***(0.5 × VREF / Gain) / (2^{23} - 1)***. Positive full-scale output code is ***7FFFFFH*** and negative full-scale output code is ***800000H***.

Table 8: Ideal Output Code vs. Input Signal

Input Signal V_{IN} (AINP - AINN)	Ideal Output Code
≥ +0.5 VREF / Gain	7FFFFFH
(+0.5 VREF / Gain) / (2^{23} - 1)	000001H
0	000000H
(-0.5 VREF / Gain) / (2^{23} - 1)	FFFFFFH
≤ -0.5 VREF / Gain	800000H

2.8 Operational Modes

- **Standby Mode:** Activated by holding SCLK HIGH after ***DRDY / DOUT*** goes low. Analog circuitry powers down while clock circuit remains active. Pulling SCLK LOW exits Standby mode.
- **Power Down Mode:** Activated by pulling ***PDWN*** LOW. All internal circuits are disabled, reducing total power consumption to under 1.6 µA.

3. Packaging Information

The CS1232 is available in a standard 24-pin TSSOP package (TSSOP-24).